Title of the Invention

CARRY SAVE ADDERS

Field of the Invention

The present invention relates to carry save adders and in particular but not exclusively to carry save adders which are able to reduce the number of partial products to two.

Background to the Invention

In digital arithmetic, partial products are obtained when two numbers are multiplied together. The number of partial products will depend on the method used for obtaining the partial products. In a conventional operation, the number of partial products may be equal to the number of bits in the multiplier. However, techniques such as Booth encoding make it possible to reduce the number of partial products obtained. For example Booth coding allows the number of partial products to be reduced by a factor of 2. The Booth encoding method is sometimes referred to as the Booth-MacSorley algorithm.

In the Booth coding method, a triplet of bits of the multiplier is input to a Booth coder which provides three outputs, the values of which depends on the input values. The outputs of the Booth coder are then used to modify bits of the number to be multiplied by the multiplier.

Carry save adders which reduce three partial products to two partial products are known. This type of carry save adder is sometimes referred to as a 3 to 2 carry save adder. Such a carry save adder is in fact a full adder. A full adder is a binary logic circuit which produces a two-bit sum where one bit represents the sum and the other bit represents the carry when

three one bit binary numbers are added together. The three one bit numbers may be corresponding bits from three partial products.

Carry save adders which reduce four partial products to two partial products are also known. This type of carry save adder is known as a 4 to 2 carry save adder. One example of such a carry save adder is shown in the IEEE Journal of Solid State circuits, Vol 30, No 3, March 1995: "A 4.4ns CMOS 54x54-b using pass-transistor multiplexer", page 251 to 257, N Ohkubo et al. This structure generally yields faster partial product compression than the use of 3 to 2 carry save adders. The 4 to 2 carry save adder actually compresses five partial products into three and is therefore sometimes referred to as a 5 to 3 carry save adder. This carry save adder is connected in such a way that four of the inputs are corresponding bits from four partial products whilst the fifth input is fed from a neighbouring adder and is known as the "carry in". The output of this carry save adder consists of one sum bit and two carry bits. One of these carry bits is input to a neighbouring carry save adder and forms one of the five inputs of that carry save adder.

Summary of the Invention

It is an aim of embodiments of the present invention to provide a carry save adder unit which is capable of compressing more than five inputs to a smaller number of outputs.

According to one aspect of the present invention, there is provided a carry save adder for reducing the number of inputs to a lower number of outputs, said carry save adder comprising four carry save adders, said four carry save adders being arranged in two layers with the first and second carry save adders being arranged in a first of said layers and the third and fourth carry save adders being arranged in a second of said layers, said third

and fourth carry save adders being arranged to provide said outputs, said third and fourth carry save adders each receiving at least one output from each of said first and second carry save adders and the first and second carry save adders being arranged to receive at least some of said inputs.

This arrangement permits a relatively short routing between the carry save adders to be achieved. This may also improve timing.

At least one of the inputs may be input to at least one of the third and fourth carry save adders.

The carry save adder circuit may be a 9 to 4 carry save adder circuit. The first carry save adder may be a 5 to 3 carry save adder and the second, third and fourth carry save adders may be 3 to 2 carry save adders. The first to fifth inputs may be input to the first carry save adder and the sixth to eighth inputs may be provided to the second carry save adder. The ninth input may be input directly to one of the third and fourth carry save adders.

The carry save adder circuit may alternatively be a 7 to 4 carry save adder circuit. The first to third carry save adders may be 3 to 2 carry save adders and the fourth carry save adder may be a half adder. The first to third inputs may be input to the first carry save adder and the fourth to sixth inputs may be provided to the second carry save adder. The seventh input may be input directly to one of the third and fourth carry save adders.

According to a second aspect of the present invention there is provided a carry save adder circuit for reducing nine inputs to four outputs, said carry save adder circuit comprising four carry save adders, the first carry save adder being a 5 to 3 carry save unit and the second, third and fourth carry save adders being 3 to 2 carry save adders.

According to a third aspect of the present invention there is provided a carry save adder circuit for reducing seven inputs to four outputs, said carry save adder circuit comprising four carry save adders, the first, second and third carry save adders being 3 to 2 carry save adders and the fourth carry save unit being a half adder.

According to a fourth aspect of the present invention there may be provided an arithmetic unit for processing a plurality of partial products, said unit comprising a plurality of carry save adder circuits as claimed in any preceding claim, wherein the inputs to each of said carry save adder circuits are provided by said plurality of partial products.

Brief Description of the Drawings

For a better understanding of the present invention and as to how the same may be carried into effect, reference will now be made by way of example to the accompanying drawings in which:

Figure 1 shows a 3 to 2 carry save adder;

Figure 2 shows a 5 to 3 carry save adder;

Figure 3 shows three 5 to 3 carry save adders connected together in series and used as 4 to 2 carry save adders;

Figure 4 shows a 9 to 4 carry save adder embodying the present invention;

Figure 5 shows a arithmetic unit embodying the present invention;

Figure 6 shows a 7 to 4 carry save adder embodying the present invention;

Figure 7 shows one possible structure of a 3 to 2 carry save adder;

Figure 8 shows one possible structure of a 5 to 3 carry save adder; and

Figure 9 shows the construction of the multiplexers of Figure 8 in more detail.

Description of the Preferred Embodiments

Reference will first be made to Figure 1 which shows a conventional 3 to 2 carry save adder 2. It should be appreciated that carry save adders are sometimes referred to as compressors. The carry save adder 2 of Figure 1 is a conventional full adder and has three inputs A, B and C. Inputs A, B and C are to be added together. The carry save adder 2 of Figure 1 has two outputs S and Cout. The first output S is the sum output and the second output Cout is the carry output. The first output S represents the least significant bit of the sum of A and B and C whilst the second output Cout represents the most significant bit of the sum of A and B and C.

The truth table for the carry save adder of Figure 1 is as follows:-

A	B	C	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 2 shows a 5 to 3 carry save adder. As mentioned hereinbefore, this carry save adder is sometimes referred to as a

4 to 2 carry save adder. The carry save adder 4 of Figure 2 has five inputs, inputs A, B, C, D and CI. A, B, C and D are to be added together along with CI which represents a carry input. Where a number of adders are connected, the input CI will be provided by the output of a preceding carry save adder.

The carry save adder 4 of Figure 2 has three outputs, the first output S, the second output C01 and the third output C02. The first output S, which is the sum output, represents the least significant bit of the sum of $A + B + C + D + CI$. The other two output signals C01 and C02 are the carry signals. These carry out signals are same as the carry out signals for a full adder except that there are two carry out signals which have the same significance (2^{i+1} if the inputs have the significance 2^i).

Reference is now made to Figure 4 which shows a 9 to 4 carry save adder 20 embodying the present invention. The carry save adder 20 embodying the present invention comprises first to fourth carry save adders 22 to 28 respectively. The first carry save adder 22 is a 5 to 3 carry save adder of the type shown in Figure 2. The second, third and fourth carry save adders 24, 26 and 28 are 3 to 2 carry save adders or full adders as shown in Figure 1.

The first carry save adder 22 receives the first five inputs 11-15. These first five inputs represent bits from the first to fifth partial products. The second carry save adder 24 receives the sixth, seventh and eighth inputs 16, 17 and 18 representing bits from the sixth to eighth partial products.

The sum output S of the first carry save adder 22 provides the third input c of the fourth carry save adder 28. The first carry output C01 of the first carry save adder 22 provides the third input c of the third carry save adder 26. The second carry output C02 of the first carry save adder 22 provides the second input b of the third carry save adder 26.

The sum output S of the second carry save adder 24 provides the second input b of the fourth carry save adder 28. The carry output CO1 of the second carry save adder 24 provides the first input a of the third carry save adder.

The third carry save adder 26 therefore receives all three of its inputs a to c from the outputs of the first and second carry save adders 22 and 24. The fourth carry save adder 28 thus has its second and third inputs b and c provided by the outputs of the first and second carry save adders 22 and 24. The first input a of the fourth carry save adder 28 is provided by the ninth input 19 from the ninth partial product.

The fourth carry save adder 28 provides a sum output S (significance 2^i) and a first carry CO2A of significance 2^{i+1}. The third carry save adder 26 generates a second carry CO2B of significance 2^{i+1} and a third carry CO4 of significance 2^{i+2}. This assumes that each of the inputs I1 to I9 have a 2^i significance.

It should be appreciated that the interconnections described in relation to Figure 4 is only one way of achieving the required function. For example the inputs of cell 26 can be swapped or the inputs of the cell 28 can be swapped.

The carry save adder 20 of Figure 4 has two inputs which are faster than the others. This has the advantage that when some of the partial products are generated later compared to others, the partial products which are generated later can be input to the faster inputs. In this way the timing differences between the partial products can be reduced or avoided. The ninth input 19 is fastest as it crosses only one cell or carry save adder. The fifth input 15 which is the carry input CI to the first carry save adder 22 is also faster than the other inputs to that same carry save adder or to the second carry save adder 24. This will

be discussed in more detail in relation to Figure 8 later.

In preferred embodiments of the present invention, the carry save adder 20 can be laid out in such a way as to reduce the number of wires crossing large distances. This is because there are only four cells and they can be arranged next to each other in a compact arrangement. With this arrangement the routing problems can be reduced as compared to structures such as the Wallace tree.

Reference is made to Figure 5 which shows a context in which the carry save adder 20 of Figure 4 can be used.

In the embodiment shown in Figure 4, a further carry save adder may be added. This further carry save adder may be a 4 to 2 carry save adder which generates two partial products. This 4 to 2 carry save adder will receive four bits of the same significance. Assuming that the carry save adder deals with bits of significance, the carry save adder will receive S from column I, the output CO2A and CO2B from the previous column I-1 and the output CO4 from the column I-2.

Figure 5 shows an arithmetic unit 30 which is arranged to multiply two numbers, X and Y together. Y is the multiplier in this case. Y has 17 bits and is subject to Booth coding. Y represents a 16 bit number with the 17th bit being a 1-bit extension: sign extension if the 16 bit data is signed, 0 extension if it is unsigned. This enables Y to be considered as a 17 bit signed data indicating if the data is signed or unsigned. The Booth coding of the Y value results in outputs which are used to modify the X values. As mentioned hereinbefore, Booth coding allows the number of partial products to be reduced. For example, if Y is 17 bits long, nine partial products will result from the multiplication of those two numbers, if Booth coding is used. The nine partial products are referred to by references P0 to P8.

Each partial product P0 to P8 has n bits. One bit from each of the partial products is input to the carry save adder 20 of Figure 4. If the mth bit of the first partial product P0 is selected, the $m-2^{th}$ bit will be selected from the second partial product P1, the $m-4^{th}$ bit selected from the third partial product P2 and so on In this scenario, the first bit in a given partial product is the least significant bit whilst the nth bit in the partial product is the most significant bit. In certain cases, there will be no bits available. For example, if m=4, the corresponding bit from the fourth partial product P3 would be m=-2. This gives a negative value. In these circumstances the value zero would be taken as the input to the carry save adder. Effectively the values of the partial products are offset so as to take into account the significance or weight of each of the partial product.

The number of carry save adders 20 which are provided is defined by the following equation:
number of bits = n + 2(p-1) where
n is the number of bits in each partial products
p is the number of partial products.

As discussed above, there are not always 9 bits. For example column 5 only has three bits. In those circumstances it is not necessary to use the 9 to 4 adder. Instead, a 3 to 2 carry save adder can be used. Accordingly, the carry save adder for each column can be selected in accordance with the number of bits which are to be added.

Each carry save adder provides four outputs as discussed in relation to Figure 4. The sum output S of the third carry save adder 26 provides one bit of a first partial product 34, the second output C02A of the third carry save adder 26 provides one bit of a second partial product 36, the first output C02B of the

fourth carry save adder 28 provides one bit of the third partial product 38 and the second output CO4 of the fourth carry save adder 28 provides one bit of a fourth partial product 40. The first output of the carry save adder 20 provides the mth position of the first partial product 34. The second and third outputs CO2A and CO2B provide the m+1th positions of the second and third partial products 36 and 38. The fourth output of the carry save adder CO4 provides the m+2th position of the fourth partial product 40. The positions to which the outputs of the carry save adder 20 are provided in the respective partial products 34 to 40 reflects their significance or weight. The outputs of adjacent carry save adders are at adjacent locations in the partial products 34 to 40.

These four partial products 34 to 40 which receive the outputs of the carry save adder 20 are input to respective 4 to 2 adders which reduce the number of partial products to two. These two partial products can then be summed to provide a single result.

Reference is now made to Figure 6 which shows a 7 to 4 carry save adder 50. The 7 to 4 carry save adder 50 comprises four carry save adders 52 to 58. The first, second and third carry save adders 52 to 56 are 3 to 2 adders, such as illustrated in Figure 1. The fourth carry save adder 58 is a half adder which receives two inputs and provides two outputs.

The first carry save adder 52 receives the first to third inputs I1, I2 and I3. The second carry save adder 54 receives the fourth fifth and sixth inputs I4, I5 and I6. The sum output S of the first carry save adder 52 provides the first input a to the third carry save adder 56. The sum output of the second carry save adder 54 provides the second input b to the third carry save adder 56. The third input to the third carry save adder 56 is provided by the seventh input I7.

The fourth carry save adder 58 receives the carry output C01 of the first and the second carry save adders which provide the first and second inputs a and b respectively.

The output of the third carry save adder provides the output S as its sum output and the output C02A as its carry output. The sum output of the fourth carry save adder 58 provides the second carry output C02B output whilst the carry output of the fourth carry save adder 58 provides the carry output C04. These outputs have the same significance or weight as those outputs of the 9 to 4 carry save adder shown in Figure 4.

The seventh input 17 is faster than the other inputs in that it only has to pass through one of the carry save adders. The first and second carry save adders 52 and 54 receive the first six inputs 11 to 16. The first and second carry save adders 52 and 54 effectively provide a first layer. The third carry save adder 56 and the half adder 58 provide a second layer and receive the respective outputs from the first layer as well as the seventh input 17. In practice, the adders making up the carry save adder of Figure 6 can be arranged in any suitable way so as to minimise the length of the connections as with the embodiment described in relation to Figure 4.

The carry save adder of Figure 6 can also be used in a similar context to that shown in Figure 5 if seven partial products are generated, particularly if seven bits are to be processed in a column. The carry save adder can also be used in the embodiment shown in Figure 5 where there are more than seven partial products but only seven bits are provided for a given column.

It should be noted that, as with the carry save adder of Figure 4, some of the interconnections between the carry save adders making up the 7 to 4 carry save adder can be altered without altering the function of the adder as a whole. For example the

inputs to the third carry save adder 56 can be swapped with other inputs to that carry save adder. Likewise the inputs to the half adder 58 can be swapped around.

Again a 4 to 2 carry save adder can be provided to reduce the number of partial products to two.

The arrangement of both the 9 to 4 and the 7 to 4 carry save adders allow short routings to be achieved between the carry save adders. This improves both timing and routing of these carry save adders. This is particularly advantageous when embodiments of the present invention are incorporated in an integrated circuit.

Reference is made to Figure 3 which shows three of the carry save adders 6a, 6b and 6c of Figure 2 connected together. Each of the 5 to 3 carry save adders 6 receives inputs A to D and the input CI from the preceding carry save adder and provides three outputs as in Figure 2. The first carry save adder block 6a receives a carry input CI from a preceding carry save adder. If there is no previous carry save adder, then input CI will be zero. The first carry save adder 6a outputs the second carry output CO2 to the second carry save adder 6b. This second carry output CO2 from the first carry save adder is the carry input CI to the second carry save adder 6b. Likewise, the second carry save adder 6b provides its second carry output CO2 as the carry input CI to the third carry save adder 6c. It should be noted that the input CI is not used to generate the CO2 output of the same carry save adder.

This means that the carry propagation is only done from one carry save adder to the next. The respective inputs A to D to each of the carry save adders 6 may represent adjacent bits from four partial products. For example, the first carry save adder 6a receives the nth bit of first, second, third and fourth partial products with the second and third carry save adders 6b and c receiving the n+1 and n+2 bits respectively of those same partial

products.

Figure 3 illustrates why the 5 to 3 carry save adder is sometimes referred to as the 4 to 2 carry save adder. In particular four inputs A, B, C and D are reduced to two outputs S and C01.

Reference will now be made to Figure 7 which shows a structure of a 3 to 2 carry save adder 81. The carry save adder 81 has three inputs A, B and C. The carry save adder 81 has first and second exclusive OR gates 80 and 82 and first to fourth NAND gates 84 to 90. The first exclusive OR gate 80 receives the first input A and the output of the second exclusive OR gate 82. The output of the first exclusive OR gate 80 provides the sum output S.

The second exclusive OR gate 82 receives the second and third inputs B and C as its two inputs.

The first NAND gate 84 receives an input from the second and third inputs B and C. The second NAND gate 86 receives its input from the first and third inputs A and C whilst the third NAND gate 88 receives its inputs from the first and second inputs A and B. The output of each of the first to third NAND gates 84 to 88 provide the inputs to the fourth NAND gate 90, the output of which provides the carry output C.

Reference is made to Figure 8 which shows one possibility for the 5 to 3 carry save adder 91.

The 5 to 3 carry save adder 91 comprises six multiplexers 92, 93, 94, 96, 98 and 99 each of which has the construction shown in Figure 9. The first multiplexer 92 receives the fourth input 14 and its inverse. An inverter 100 is provided for inverting the fourth input 14. The first multiplexer 92 also receives the third input 13 as a select signal.

The second multiplexer 93 receives the second signal 12 and its inverse. A second inverter 102 is provided for inverting the second input 12. The select signal is provided by the first input 11. The third multiplexer 94 receives the first and third inputs 11 and 13 and the output of the second multiplexer 93 provides its select signal. The output of the third multiplexer 94 is input to a first buffer 104. The output of the first buffer 104 provides the second carry output CO2.

The fourth multiplexer 96 receives the output of the first multiplexer 92 and its inverse. A third inverter 106 is provided for inverting the output of the first multiplexer 92. The output of the second multiplexer 93 provides the select signal for the fourth multiplexer 96.

The fifth multiplexer 98 receives the carry input Ci and the fourth input 14 as inputs and the output of the fourth multiplexer 96 as the select signal. The output of the fifth multiplexer 98 is input to a second buffer 108, the output of which provides the first carry output CO1.

The final multiplexer 99 receives the carry input Ci and its inverse. A fourth inverter 110 is provided to provide the inverse of the carry input cl. The select signal is provided by the output of the fourth multiplexer 96. The output of the sixth multiplexer is input to a third buffer 112, the output of which provides the sum output S.

The arrangement of Figure 8 shows that the input Ci has less gate levels to cross that the inputs I1, I2, I3 and I4 and is therefore faster than these latter inputs.

Reference is made to Figure 9 which shows the construction of the multiplexers of Figure 8 in more detail. The inputs to the multiplexer 149 are X and Y whilst the select signal is Z. The

multiplexer 149 comprises four pairs of transistors 150 to 156. Each pair of transistors comprises a p-type transistor 120 to 126, and a n-type transistor 128 to 134 respectively.

In the first pair of transistors 150, the p-type transistor 120 receives the select signal Z whilst the n-type transistor 128 receives the inverse of the select signal Z. This arrangement also applies to the third pair of transistors 154 comprising of the third p-type transistor 124 and the third n-type transistor 132.

The second and fourth pairs of transistors 152 and 156 are such that the n-type transistors 130 and 134 receive the select signal Z whilst the p transistors 124 and 126 respectively receive the inverse of the select signal Z.

The circuitry for the carry save adders is by way of example only and any other suitable circuitry can be used.

Embodiments of the present invention may be incorporated in a digital signal processor. Embodiments of the present invention may be incorporated in an integrated circuit.